

REMARKS

Claims 1-20 have been presented for examination in the above-identified U.S. Patent Application.

5

Claims 1-20 have been rejected in Office Action dated May 24, 2004.

Claims 1 and 8 have been amended by this Amendment
10 A.

15

Claims 1-20 are still in the Application and reconsideration of the Application is hereby respectfully requested.

20

Referring to Paragraph No. 2 of Page 2 of Office Action dated May 24, 2004, the Abstract of the Disclosure has been objected to because of cited informalities and the presence of two versions of the Abstract. One version of the Abstract has been deleted. The informalities cited by Examiner have been corrected in the remaining version. Therefore, these objections to the Specification have been answered by Amendment.

25

Referring to Paragraph No. 3 of Page 2 of Office Action dated May 24, 2004, the updated Patent Application Numbers for the Related Applications have been provided by amendment to the Related Applications section.

30

Referring to Paragraph No. 4 of Page 2 of Office Action dated May 24, 2004, the Specification has been reviewed. Some minor errors have been corrected by this Amendment A.

Referring to Paragraph No. 5 of Page 2 and continuing through Paragraph 7 of Office Action dated May 24, 2004, Claims 1-20 have been provisionally rejected under the doctrine of obviousness double patenting. As indicated by Examiner, responses to the double patenting rejection, such as the terminal disclaimer, are available. However, because these rejections are provisional, at present, i.e., no Claim having been allowed in either the present Application or the referenced Applications, Applicant prefers to place this matter in abeyance pending the outcome of the prosecution of the Application and/or the references.

Referring to Paragraph Nos. 9-12, Claims 1-20 have been rejected under 35 U.S.C. 102 (b) as being anticipated by U.S. 5,845,153 issued in the name of Sun et al (hereinafter referred to as Sun). Before directly addressing the rejection, the invention disclosed by the Application will be summarized. The Utopia protocol implements a procedure for transferring data between data processing machines. A Utopia-protocol interface is needed to interface between the data processing systems. In the present invention, the Utopia interface interfaces with the direct memory access unit of the processor. Fig.8 provides an implementation for the Utopia interface (18) to interact with the direct memory access unit (14). The direct memory access unit provides for independent access by central processing unit, the main memory unit, peripherals and other components without intervention by the central processing unit, i.e., the central processing unit's main responsibility is the processing of data in the main memory unit as soon as possible. In the situation described in the Application, the central processing unit is a digital signal processing unit, a

high specialized processor used for calculation-intensive programs typically under the control of a host processor. In this situation, the direct memory access unit can not permit any delay in providing data to the central
5 processing unit of the digital signal processing unit. Consequently, the Utopia interface unit must not only reformat the packets sent in the Utopia format, but must provide a buffer memory between the relatively slow clock speed of the bus transmitting the data to and from the
10 digital signal processing unit and the high clock speed of the direct memory access unit. In the independent Claims in the Application, Claims 1 and 8 have been amended to specifically point out that the Utopia interface exchanges data with the direct memory access
15 unit of the DSP. In the other independent Claim 12, this configuration is specifically pointed out in the Claim preamble.

Turning now to the Sun reference, this reference
20 describes a Utopia-protocol interface; however, the interface shown in Fig. 1 is between communication bus labeled PHY 170 (To Network) and a PCI bus. In addition, the PCI bus in Fig. 1 is designated 32 MHz, 32-Bit multiplexed bus. This designation clearly indicates that
25 the Sun reference does not contemplate a high speed data transfer. The Sun invention addresses limitations in memory space and uses a buffer to accommodate various physical limitations in the memory unit. In contradistinction, the present invention uses the Utopia
30 interface to provide a buffer between the communication bus and the direct memory access unit for the accommodation of the difference in rate data transfer, a difference not contemplated by the Sun reference.

Expressed in another manner, both the present invention and the reference describe an interface the communication bus and a data processing system. However, in the Sun reference, the buffering is with respect to
5 memory space, and the Specification describes an implementation that results in the appropriate memory space buffering. In the present invention, the Specification, in conjunction with the Figures, describe a Utopia interface unit that buffers the data rate
10 transfer between the communication bus and the data processing unit. The control signals that permit the coupling of the communication bus through the Utopia interface unit to the direct memory access unit. These differences between the Application and reference are
15 clearly evident in the Claims. Both the Utopia interface unit of the reference and the Utopia interface unit of the invention operate in a completely independent manner, linked only by the common use of the Utopia protocol.

20 Therefore, rejection of Claims 1-20 under 35 U.S.C. 102(b) as being anticipated by the Sun reference is respectfully traversed, In addition, a possible rejection under 35 U.S.C. 103 as being unpatentable in view of the Sun reference would be traversed because of
25 the differences in the function of the two Utopia interface units cited above.

CONCLUSION

In view of the foregoing discussion and the foregoing amendments, it is believed that Claims 1 - 20 are now in condition for allowance of Claims 1 - 20 is respectfully requested. Applicants hereby respectfully request a timely Notice of Allowance be issued for this Application.

Respectfully submitted,



William W. Holloway
Attorney for Applicants
Reg. No. 26,182

Texas Instruments Incorporated
PO Box 655474, MS 3999
Dallas, TX 75265
(281) 274-4064